transmitting an output clock signal.

2. **(Original)** The method of claim 1, wherein inducing the phase build-out activity includes eliminating a set of input transients.

3. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to manage a plurality of phase-locked loops.

4. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock normal state

5. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock freerun state.

6. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to set the main clock to a main clock holdover state.

7. **(Original)** The method of claim 6, further comprising activating the phase buildout activity.

8. **(Original)** The method of claim 6, further comprising applying a frequency history to a frequency synthesizer in the main clock.

9. **(Original)** The method of claim 8, wherein applying the frequency history includes applying an approximately twenty-five second frequency history.

10. **(Original)** The method of claim 8, further comprising forcing a phase measurement circuit into a zero phase error state by preloading a phase measurement counter with a zero substantially on an edge of an input signal.

11. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to select a short time constant filter in the main clock.

12. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to select a long time constant filter in the main clock.

13. **(Original)** The method of claim 1, further comprising utilizing the stratum clock state machine to select a programmable filter.

14. **(Original)** The method of claim 1, further comprising providing the stratum clock state machine with a user selection input, wherein the user selection input includes at least one member selected from the group consisting of: a select freerun mode, a select reference A mode, a select reference B mode and a select holdover mode.

15. **(Original)** The method of claim 1, further comprising setting the stratum clock state machine in a state including at least one member selected from the group consisting of: a stratum clock state machine normal state, a stratum clock state machine freerun state, a stratum clock state machine switch state, a stratum clock state machine offset state and a stratum clock state machine holdover state.

16. **(Original)** The method of claim 1, further comprising providing the stratum clock state machine with a frequency offset input including:

receiving a frequency offset signal produced by each of a pair of input digital phase-locked loops; and

measuring the frequency offset signal.

17. **(Original)** The method of claim 16, further comprising setting the stratum clock state machine to the stratum clock state machine offset state if a measured frequency offset signal is greater than approximately 2.4 parts per million.

18. **(Original)** The method of claim 17, further comprising maintaining the stratum clock state machine offset state for approximately an additional 12 seconds after the measured frequency offset signal is de-asserted.

19. **(Original)** The method of claim 1, further comprising providing the stratum clock state machine with a frequency error input including:

receiving a frequency error signal produced by each of the pair of input digital phase-locked loops; and

measuring the frequency error signal.

20. **(Original)** The method of claim 19, further comprising setting the stratum clock state machine to a stratum clock state machine holdover state if a measured frequency error signal is greater than approximately 14.4 parts per million.

21. **(Original)** The method of claim 20, further comprising applying an approximately twenty-five second frequency history to the frequency synthesizer in the main clock.

22. **(Original)** The method of claim 1, further comprising providing the stratum clock state machine with a phase step input including:

receiving a phase step signal produced by each of the pair of input digital phase-locked loops; and

measuring the phase step signal.

23. **(Original)** The method of claim 22, further comprising setting the stratum clock state machine to the stratum clock state machine holdover state if a measured phase step signal is greater than approximately 1.4 microseconds.

24. **(Original)** The method of claim 23, further comprising performing a phase buildout

function for approximately 12 seconds.

25. **(Original)** The method of claim 1, further comprising providing a set of three timers, wherein each timer is set by a state machine input event, including: a phase buildout timer, a hold timer, and a skip timer.

26. **(Original)** The method of claim 25, further comprising clearing the set of three timers when a reference switch is detected.

27. **(Original)** A computer program, comprising computer or machine readable program elements translatable for implementing the method of claim 1.

28. **(Original)** An apparatus for performing the method of claim 1.

29. **(Original)** A field programmable gate array for performing the method of claim 1.

30. **(Original)** An application specific integrated circuit for performing the method of claim 1.

31. **(Cancelled)**

32. **(Cancelled)**

33. **(Cancelled)**

34. **(Cancelled)**

35. **(Cancelled)**

36. **(Cancelled)**

37. **(Cancelled)**

38. **(Cancelled)**

39. **(Cancelled)**

40. **(Cancelled)**

41. **(Cancelled)**

42. **(Cancelled)**

43. **(Cancelled)**

44. **(Cancelled)**

45. **(Cancelled)**

46. **(Cancelled)**

47. **(Cancelled)**

48. **(Cancelled)**